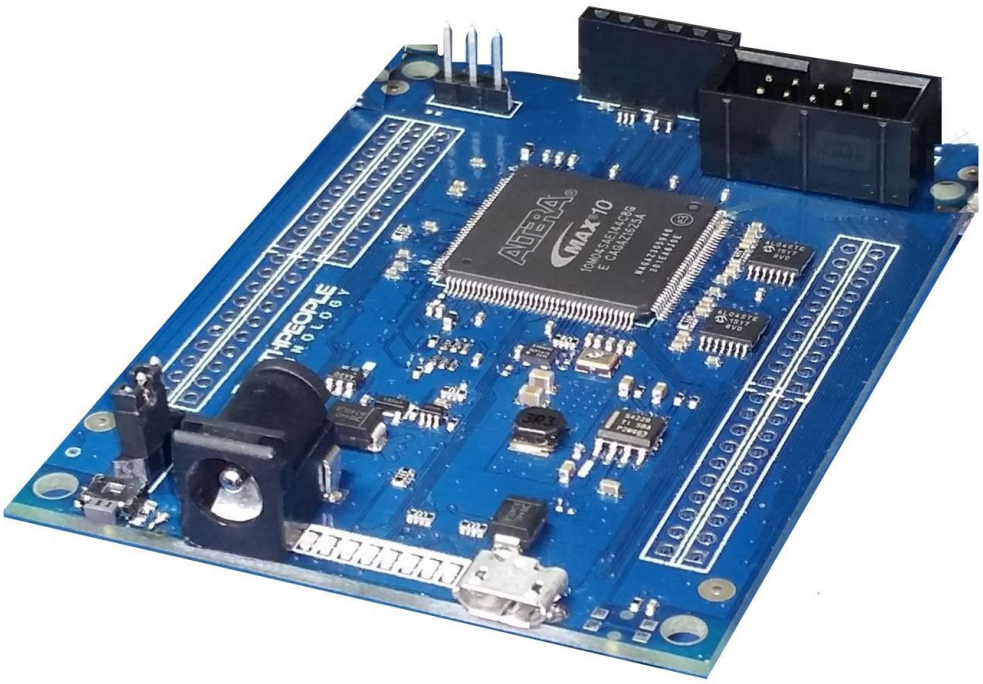
MAXPROLOGIC

FPGA DEVELOPMENT SYSTEM

Data Sheet



The MaxProLogic is an FPGA development board that is designed to be user friendly and a great introduction into digital design for anyone.

The MaxProLogic is an FPGA development board that is designed to be user friendly and a great introduction into digital design for anyone. The core of the MaxProLogic is the Altera MAX10 FPGA. This powerful chip has 4,000 Logic Elements and 200Kbits of Memory. The MAX10 is

easily scalable from the entry level college student to the most advanced projects like an audio sound meter with FFT. Upon the many great features of the MaxProLogic is the MAX10 chip has a built in Flash for configuration and incorporates 8 channels of Analog to Digital Conversion. These two features alone create a far superior FPGA chip than any competitor on the market. It allows the user to create more diverse projects.

- MAX 10 10M04SA FPGA FROM INTEL/ALTERA
- 4,000 Logic Elements; 2.2 Mbit On chip Flash; 189 Kbit On Chip SRAM
- 8 Analog Input Channels; 12 bit; 1MSamples/Second
- 65 Available I/O's at connectors
- 8 Green User configurable LEDs
- 1 Power Pushbutton Switch; 1 User Configurable Pushbutton Switch
- On Board SD Card Slot
- Two Power options: Standard USB (+5V @ 2Amp) Using Micro-B connector;
- 5mm Barrel Connector Accepts +9V @ 3Amp
- Switching Power Supply, Provides stable output under high load stress
- Two Clocks: 50MHz Oscillator; 32.768KHz Oscillator
- On board interface to Standard USB to Serial Adapters

1 Block Diagram

Figure 1 MaxProLogic Component Location

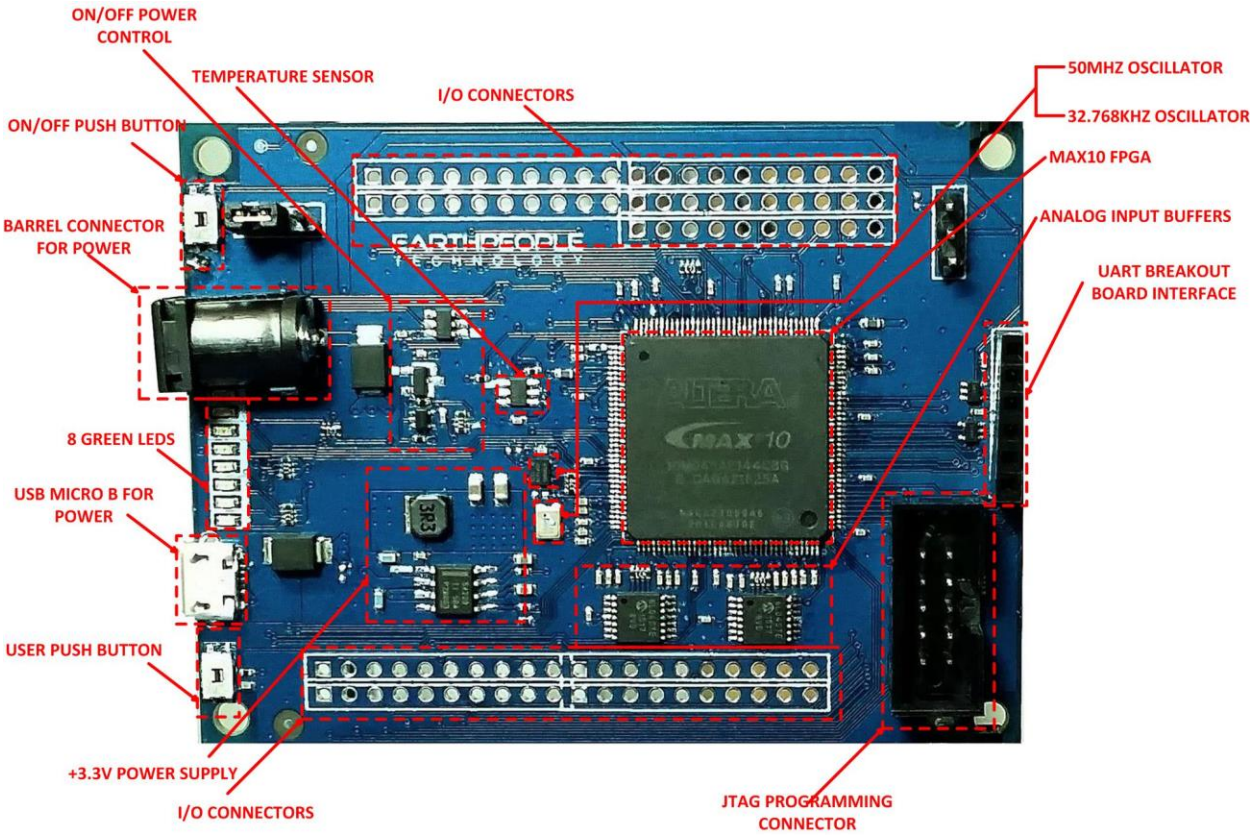
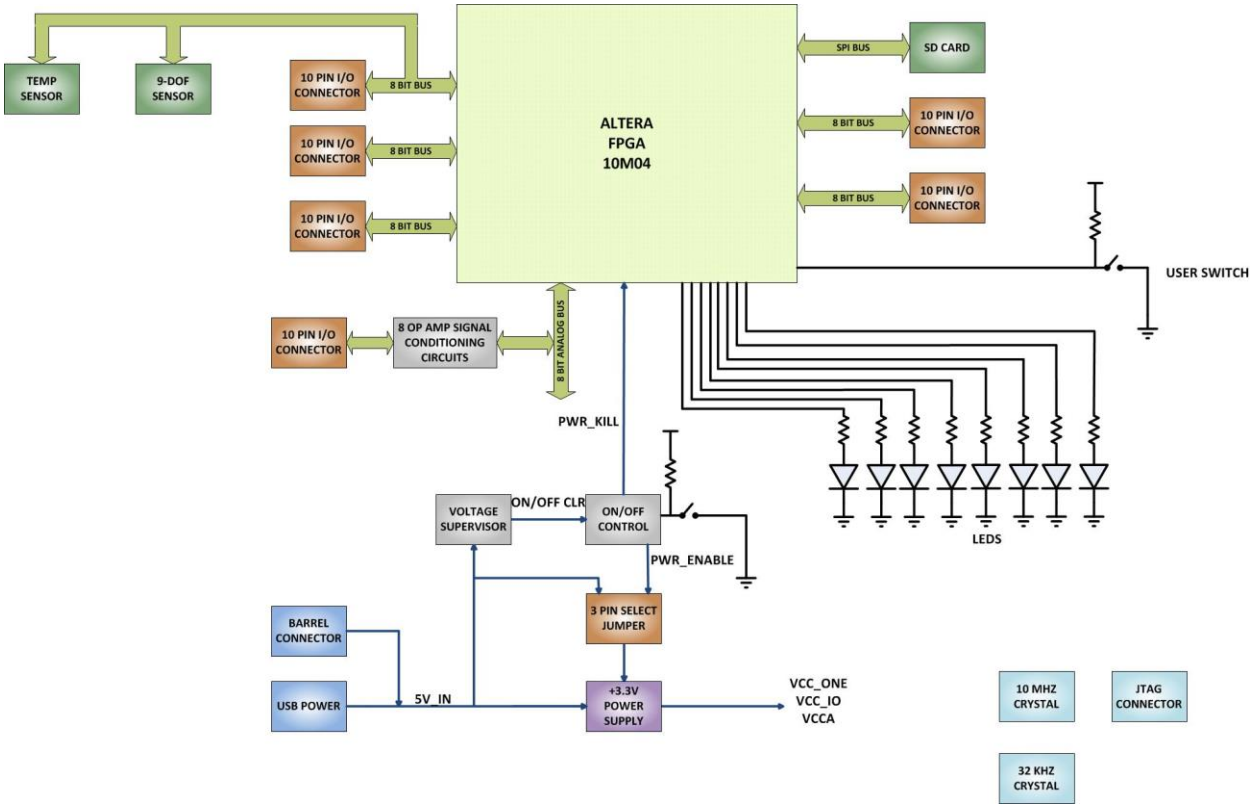
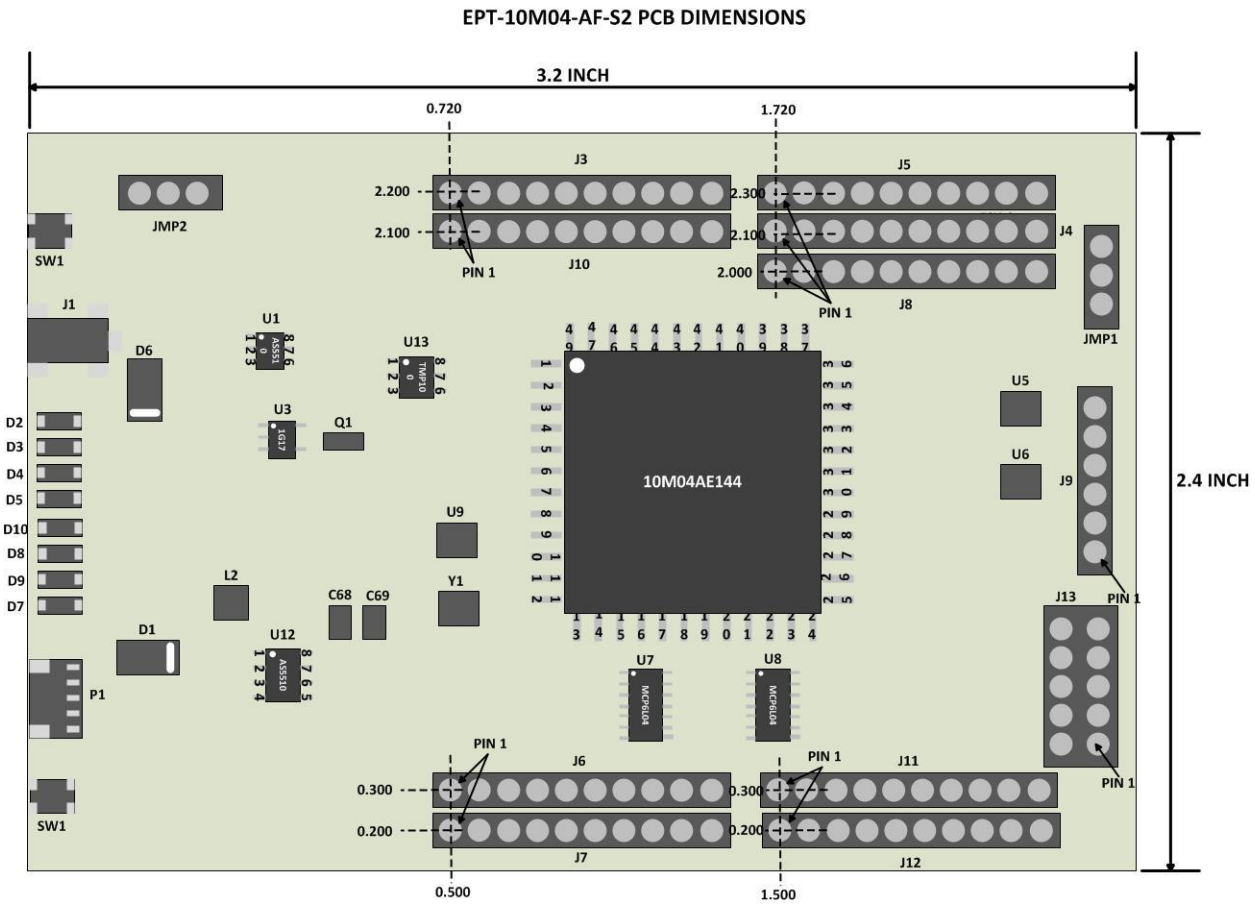


Figure 2 EPT-4CE6-AF Block Diagram


TEMP SENSOR
9-DOF SENSOR
10 PIN I/O CONNECTOR
8 BIT BUS
10 PIN I/O CONNECTOR
8 BIT BUS
10 PIN I/O CONNECTOR
8 BIT BUS
ALTERA FPGA 10M04
SPI BUS
SD CARD
8 BIT BUS
10 PIN I/O CONNECTOR
8 BIT BUS
10 PIN I/O CONNECTOR
USER SWITCH
10 PIN I/O CONNECTOR
8 OP AMP SIGNAL CONDITIONING CIRCUITS
8 BIT ANALOG BUS
PWR_KILL
VOLTAGE SUPERVISOR
ON/OFF CLR
ON/OFF CONTROL
PWR_ENABLE
LEDS
BARREL CONNECTOR
3 PIN SELECT JUMPER
USB POWER
5V_IN
+3.3V POWER SUPPLY
VCC_ONE
VCC_IO
VCCA
10 MHZ CRYSTAL
JTAG CONNECTOR
32 KHZ CRYSTAL

2 Mechanical Dimensions



3 Pin Mapping

Figure 4. Pin Mapping between Arduino Due, DueProLogic and FPGA User code

Connector-Pin #	Net Name	MAX10 Pin Number	User Code Signal Name
J3-1	XIO3_0	88	XIO3[0]
J3-2	XIO3_1	89	XIO3[1]
J3-3	XIO3_2	90	XIO3[2]
J3-4	XIO3_3	91	XIO3[3]

J3-5	XIO3_4	96	XIO3[4]
J3-6	XIO3_5	98	XIO3[5]
J3-7	XIO3_6	80	XIO3[6]
J3-8	XIO3_7	97	XIO3[7]
J3-9	GND	NC	NC
J3-10	GND	NC	NC

Connector-Pin #	**Net Name**	**MAX10 Pin Number**	**User Code Signal Name**
J4-1	COMMS_TX	92	XIO8[0]
J4-2	COMMS_RX	93	XIO8[1]
J4-3	XIO8_2	99	XIO8[2]
J4-4	XIO8_3	100	XIO8[3]
J4-5	XIO8_4	101	XIO8[4]
J4-6	XIO8_5	102	XIO8[5]
J4-7	XIO8_6	105	XIO8[6]
J4-8	XIO8_7	106	XIO8[7]
J4-9	GND	NC	NC
J4-10	GND	NC	NC

Connector-Pin #	**Net Name**	**MAX10 Pin Number**	**User Code Signal Name**
J5-1	5V_IN	NC	XIO4[0]
J5-2	3V3	NC	XIO4[1]

J5-3	XIO4_0	41	XIO4[2]
J5-4	XIO4_1	43	XIO4[3]
J5-5	XIO4_2	44	XIO4[4]
J5-6	XIO4_3	45	XIO4[5]
J5-7	XIO4_4	46	XIO4[6]
J5-8	XIO4_5	47	XIO4[7]
J5-9	GND	NC	NC
J5-10	GND	NC	NC

Connector-Pin #	**Net Name**	**MAX10 Pin Number**	**User Code Signal Name**
J6-1	SD_DAT0	48	XIO1[0]
J6-2	SD_DAT1	61	XIO1[1]
J6-3	XIO1_2	62	XIO1[2]
J6-4	XIO1_3	64	XIO1[3]
J6-5	XIO1_4	65	XIO1[4]
J6-6	XIO1_5	66	XIO1[5]
J6-7	XIO1_6	69	XIO1 [6]
J6-8	XIO1_7	70	XIO1[7]
J6-9	GND	NC	NC
J6-10	GND	NC	NC

Connector-Pin #	**Net Name**	**MAX10 Pin Number**	**User Code Signal Name**

J7-1	XIO5_0	50	XIO5[0]
J7-2	XIO5_1	52	XIO5[1]
J7-3	XIO5_2	54	XIO5[2]
J7-4	XIO5_3	55	XIO5[3]
J7-5	XIO5_4	56	XIO5[4]
J7-6	XIO5_5	57	XIO5[5]
J7-7	XIO5_6	58	XIO5[6]
J7-8	XIO5_7	59	XIO5[7]
J7-9	GND	NC	NC
J7-10	GND	NC	NC

Connector-Pin #	**Net Name**	**MAX10 Pin Number**	**User Code Signal Name**
J8-1	I2C_0_SCL	110	XIO7[0]
J8-2	I2C_0_SDA	111	XIO7[1]
J8-3	XIO7_2	113	XIO7[2]
J8-4	XIO7_3	114	XIO7[3]
J8-5	XIO7_4	118	XIO7[4]
J8-6	XIO7_5	119	XIO7[5]
J8-7	XIO7_6	112	XIO7[6]
J8-8	XIO7_7	123	XIO7[7]
J8-9	GND	NC	NC
J8-10	GND	NC	NC

Connector-Pin #	Net Name	MAX10 Pin Number	User Code Signal Name
J10-1	XIO6_0	120	XIO6 [1]
J10-2	XIO6_1	124	XIO6[1]
J10-3	XIO6_2	127	XIO6[2]
J10-4	XIO6_3	130	XIO6[3]
J10-5	XIO6_4	131	XIO6[4]
J10-6	XIO6_5	132	XIO6[5]
J10-7	XIO6_6	135	XIO6[6]
J10-8	XIO6_7	140	XIO6[7]
J10-9	GND	NC	NC
J10-10	GND	NC	NC

Connector-Pin #	Net Name	MAX10 Pin Number	User Code Signal Name
J11-1	5V_IN	NC	NC
J11-2	ANALOG_1	6	ANALOG[0]
J1-3	ANALOG_2	7	ANALOG[1]
J11-4	ANALOG_3	8	ANALOG[2]
J11-5	ANALOG_4	10	ANALOG[3]
J11-6	ANALOG_5	11	ANALOG[4]
J11-7	ANALOG_6	12	ANALOG[5]
J11-8	ANALOG_7	13	ANALOG[6]
J11-9	ANALOG_8	14	ANALOG[7]

J11-10	GND	NC	

Connector-Pin #	Net Name	MAX10 Pin Number	User Code Signal Name
J12-1	XIO2_0	74	XIO2[0]
J12-2	XIO2_1	75	XIO2[1]
J12-3	XIO2_2	76	XIO2[2]
J12-4	XIO2_3	77	XIO2[3]
J12-5	XIO2_4	78	XIO2[4]
J12-6	XIO2_5	79	XIO2[5]
J12-7	XIO2_6	81	XIO2[6]
J12-8	XIO2_7	84	XIO2[7]
J12-9	XIO2_8	85	XIO2[8]
J12-10	XIO2_9	86	XIO2[9]

4 Pushbutton switches

There are two pushbutton switches on the MaxProLogic. Both are momentary contact switches. They include a 1uF cap to ground to debounce both switches.

5 LEDs

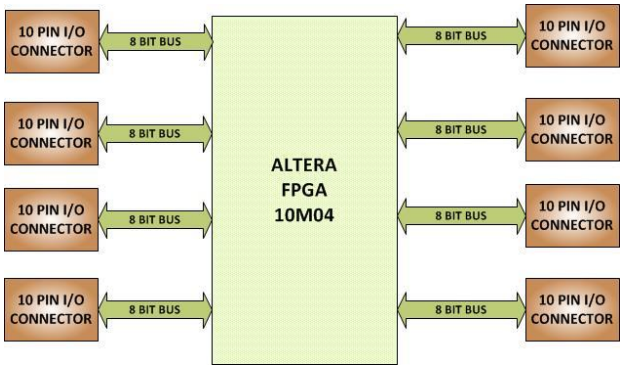
There are 8 total LEDs on the MaxProLogic. All eight are green LEDs.

Component	Net Name	Pin on FPGA	Signal in EPT Project Pinout

LED1	LED1	21	LED[0]
LED2	LED2	22	LED[1]
LED3	LED3	24	LED[2]
LED4	LED4	25	LED[3]
LED5	LED5	32	LED[4]
LED6	LED6	33	LED[5]
LED7	LED7	38	LED[6]
LED8	LED8	39	LED[7]

6 Inputs/Outputs

The MaxProLogic has eight 10 pin headers that provide 64 digital Inputs and Outputs. All of the I/O's are +3.3 VDC only. All I/O's connect directly from the FPGA to one of the ten pin headers.



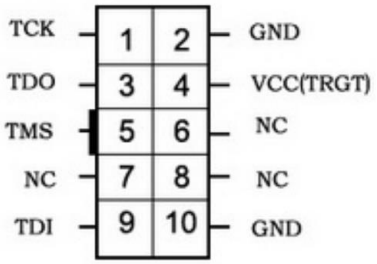
All I/O's are organized into separate banks of the FPGA. There are eight banks. These different banks provide different output speed technologies. Programmable Open Drain The optional open-drain output for each I/O pin is equivalent to an open collector output. If it is configured as an open drain, the logic value of the output is either high-Z or logic low. Use an external resistor to pull the signal to a logic high. Programmable Bus Hold Each I/O pin provides an optional bus-hold feature that is active only after configuration. When the device enters user mode, the bus-hold circuit captures the value that is present

on the pin by the end of the configuration. The bus-hold circuitry holds this pin state until the next input signal is present. Because of this, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated. For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the VCCIO level. If you enable the bus-hold feature, you cannot use the programmable pull-up option. To configure the I/O pin for differential signals, disable the bus-hold feature. Programmable Pull-Up Resistor Each I/O pin provides an optional programmable pull-up resistor during user mode. The pull-up resistor weakly holds the I/O to the VCCIO level. If you enable the weak pull-up resistor, you cannot use the bus-hold feature. Programmable Current Strength You can use the programmable current strength to mitigate the effects of high signal attenuation that is caused by a long transmission line or a legacy backplane.

7 FPGA Configuration

The MaxProLogic has an internal Flash. This flash is used to configure the FPGA. The has a 5x2 header for use in programming the MAX10 FPGA via JTAG. The connector is located in the bottom right corner of the MaxProLogic. It is shrouded and keyed to allow easier insertion.

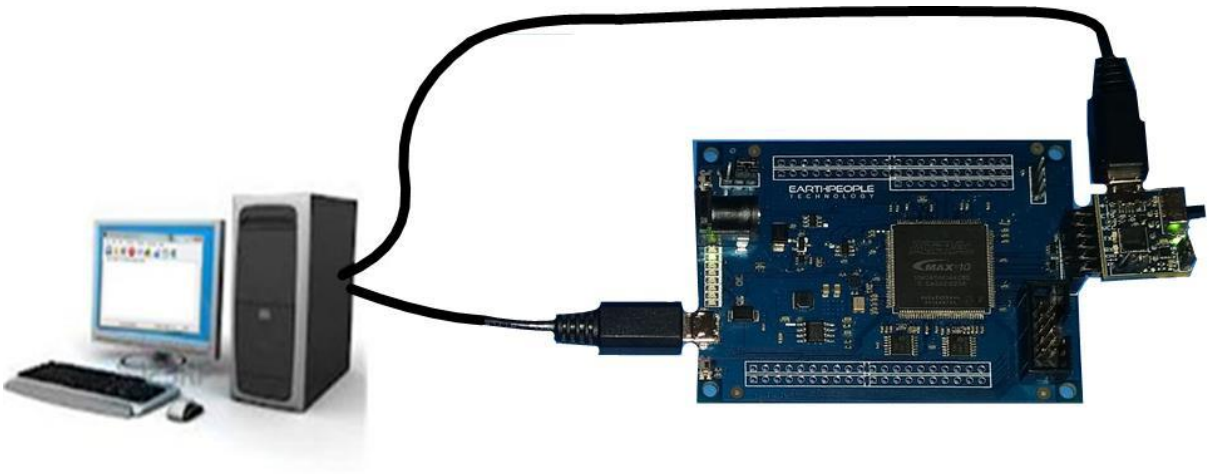
This connector uses the standard Altera Blaster connector pinout.



8 Communications Interface

The MaxProLogic is equipped with a communications port that is compatible with FTDI Breakout Boards. It is a 6 pin female header that connects directly with most Breakout boards. The pinout:

Communications Pin #	**Signal**
1	NC
2	RX
3	TX
4	VCC
5	NX
6	GND



The Communications Connector provides a path between the FTDI Breakout Board and the MAX10 FPGA. It brings both the RX and TX signals into the FPGA at the following pins.

FPGA Pin #	Signal
92	RX
93	TX

9 MaxProLogic Power

1.1.1 Core Board Power Budget

Device	Part Number	+1.2V Power	+2.5V Power	+3.3V Power
FPGA	10M04SAE144C8	??? Defined by user code. EPT-Transfer-Demo code: 50mA	10mA	??? Defined by user code. . EPT-Transfer-Demo code: 50mA

On/Off Controller	MAX1605			
Temperature Chip	TMP100			
50MHz Oscillator	FXO-HC536R-66			47 mA
32.768KHz Oscillator	FXO-HC536R-100			47 mA
Op-Amp driver	MCP6L04			0.5 mA (all four amps active)
User LEDs				20 mA
Total		**50mA**	**10mA**	**261mA**

*Theoritical Values only. This data needs to be validated