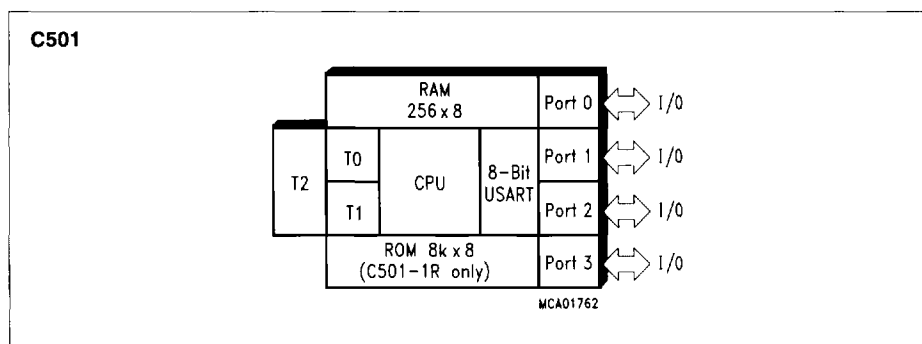


Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12/24/40 MHz operating frequency
- 8 K × 8 ROM (C501-1R only)
- 256 × 8 RAM
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- P-DIP-40, P-LCC-44 package, and P-MQFP-44
- Temperature ranges:

SAB-C501G	T_A : 0 °C to 70 °C
SAF-C501G	T_A : - 40 °C to 85 °C
SAF-C501G	T_A : - 40 °C to 110 °C (on request)



The C501-L/C501-1R described in this document is compatible with the SAB 80C32/C52 and can be used for all present SAB 80C52 applications.

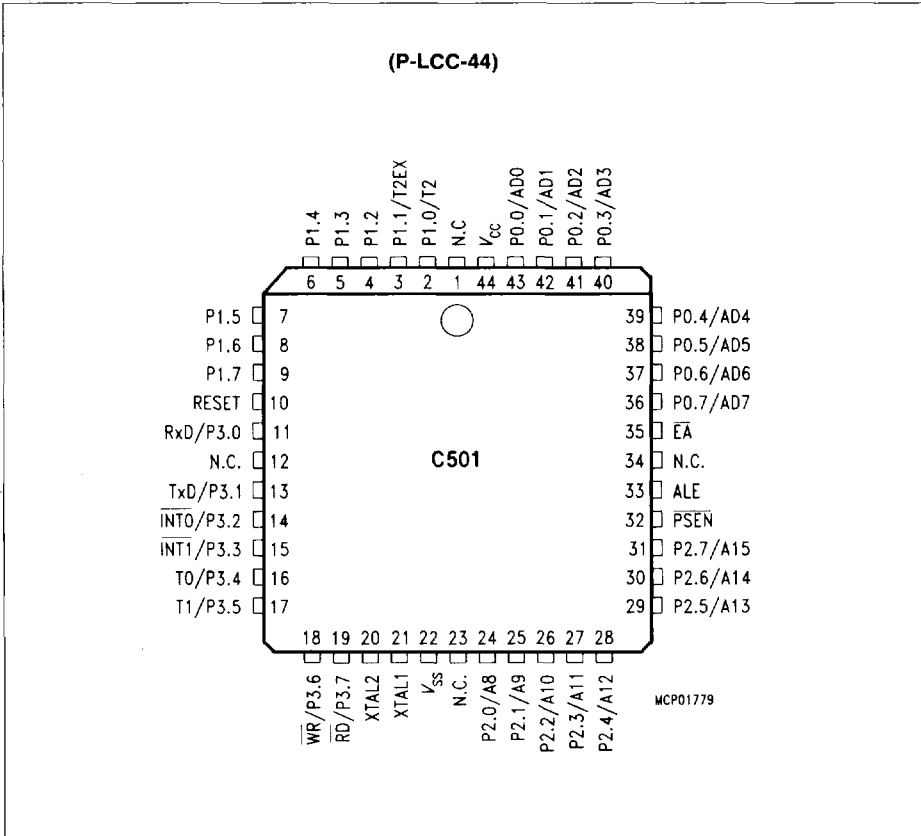
The C501-1R contains a non-volatile 8K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, four ports, three 16-bit timers counters, a seven source, two priority level interrupt structure and a serial port. The C501-L is identical, except that it lacks the program memory on chip. Therefore, the term C501 refers to both versions within this specification unless otherwise noted. Further, the term C501 refers to all versions which are available in the different temperature ranges, marked with SAB-C501G.... or SAF-C501G....

Ordering Information

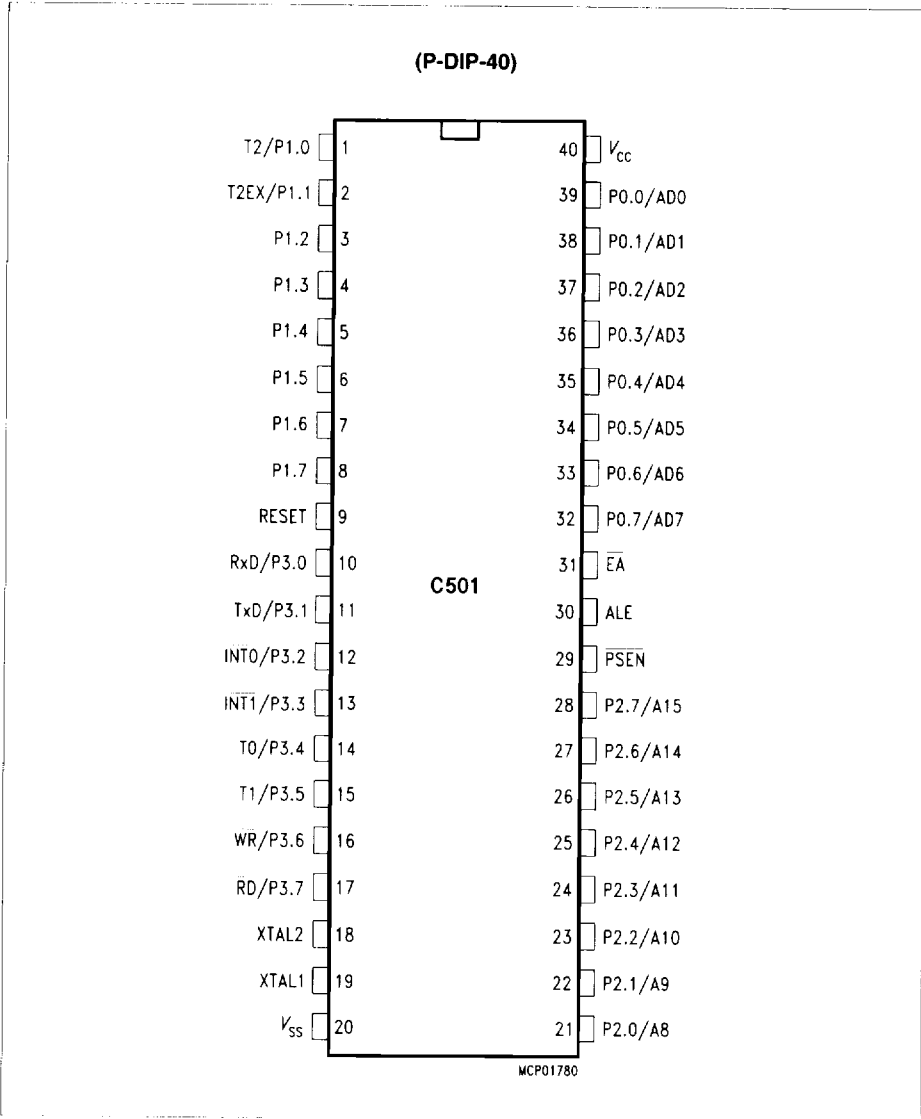
Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501G-LN SAB-C501G-LP SAB-C501G-LM	Q67120-C0969 Q67120-C0968 Q67126-C0970	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (12 MHz)
SAB-C501G-1RN SAB-C501G-1RP SAB-C501G-1RM	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (12 MHz)
SAB-C501G-L24N SAB-C501G-L24P SAB-C501G-L24M	Q67120-C1001 Q67120-C0999 Q67126-C1014	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (24 MHz)
SAB-C501G-1R24N SAB-C501G-1R24P SAB-C501G-1R24M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (24 MHz)
SAB-C501G-L40N SAB-C501G-L40P SAB-C501G-L40M	Q67120-C1002 Q67120-C1000 Q67126-C1009	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (40 MHz)
SAB-C501G-1R40N SAB-C501G-1R40P SAB-C501G-1R40M	Q67120-DXXX Q67120-DXXX Q67126-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (40 MHz)
SAF-C501G-LN SAF-C501G-LM	Q67120-C1013 Q67127-C1041	P-LCC-44 P-MQFP-44	for external memory (12 MHz) ext. temp. – 40 °C to 85 °C
SAF-C501G-LN SAF-C501G-LP	Q67120-C1010 Q67120-C1011	P-LCC-44 P-DIP-40	for external memory (24 MHz) ext. temp. – 40 °C to 85 °C
SAF-C501G-L40N	Q67126-C1051	P-LCC-44	for external memory (40 MHz) ext. temp. – 40 °C to 85 °C

Note: Versions for extended temperature range – 40 °C to 110 °C (SAH-C501G) on request.
The ordering number of ROM types (DXXX extensions) is defined after program release (verification) of the customer.

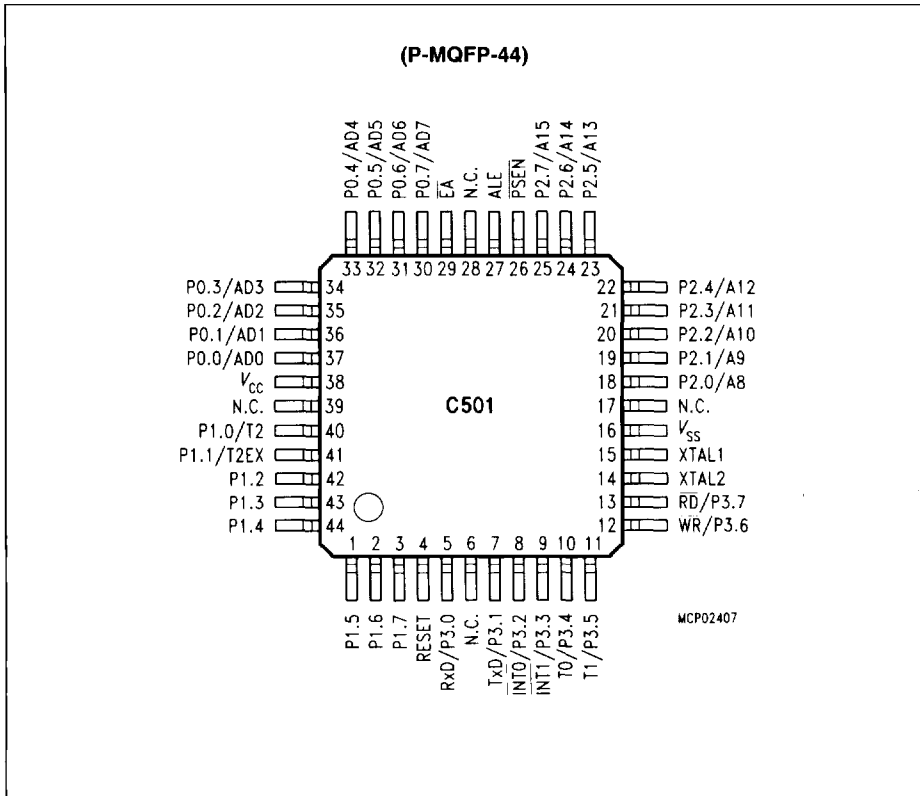
Pin Configuration
(top view)

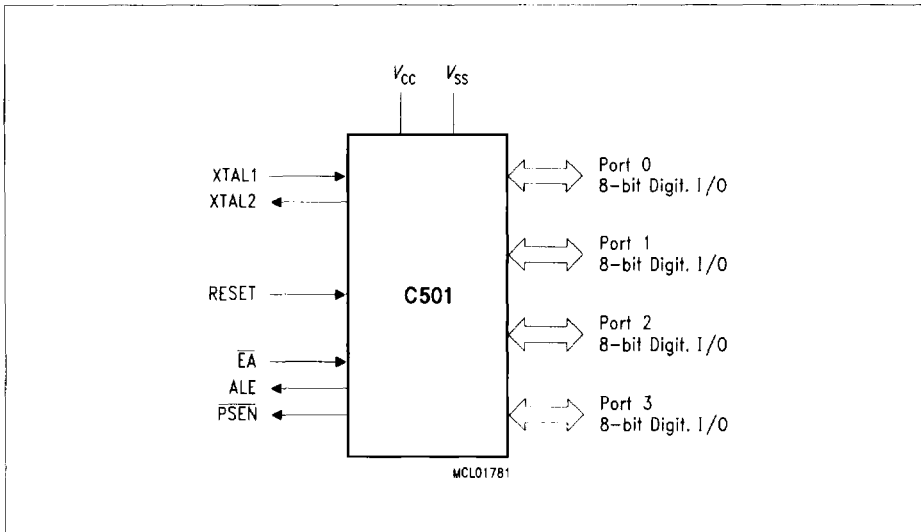


Pin Configuration
(top view)



Pin Configuration
(top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 – P1.7	2–9	1–8	40–44, 1–3,	I/O	<p>Port 1 is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be pro-grammed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 1, as follows:</p> <p>P1.0 T2 Input to counter 2 P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count</p>
	2	1	40		
	3	2	41		

*) 1 = Input
0 = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P3.0 – P3.7	11, 13–19	10–17	5, 7–13	I/O	<p>Port 3 is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate.</p> <p>The secondary functions are assigned to the pins of port 3, as follows:</p>
	11	10	5		P3.0 \overline{RxD} receiver data input (asynchronous) or data input output (synchronous) of serial interface 0
	13	11	7		P3.1 \overline{TxD} transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 $\overline{INT0}$ interrupt 0 input/timer 0 gate control
	15	13	9		P3.3 $\overline{INT1}$ interrupt 1 input/timer 1 gate control
	16	14	10		P3.4 $\overline{T0}$ counter 0 input
	17	15	11		P3.5 $\overline{T1}$ counter 1 input
	18	16	12		P3.6 \overline{WR} the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 \overline{RD} the read control signal enables the external data memory to port 0

*) 1 = Input
0 = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL2	20	18	14	–	XTAL2 Output of the inverting oscillator amplifier.
XTAL1	21	19	15	–	XTAL1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	18–25	I/O	Port 2 is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL} , in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
PSEN	32	29	26	O	The Program Store Enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
RESET	10	9	4	I	RESET A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC} .
ALE	33	30	27	O	The Address Latch Enable output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
\overline{EA}	35	31	29	I	External Access Enable When held at high level, instructions are fetched from the internal ROM (C501-1R only) when the PC is less than 2000H. When held at low level, the C501 fetches all instructions from external program memory. For the C501-L this pin must be tied low.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P0.0 – P0.7	43–36	39–32	37–30	I/O	<p>Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the C501-1R. External pull-up resistors are required during program verification.</p>
V_{SS}	22	20	16	–	Circuit ground potential
V_{CC}	44	40	38	–	Supply terminal for all operating modes
N.C.	1, 12, 23, 34	–	6, 17, 28, 39	–	No connection

Functional Description

The C501 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the SAB 80C52. While maintaining all architectural and operational characteristics of the SAB 80C52, the C501 incorporates some enhancements in the Timer2 Unit.

Figure 1 shows a block diagram of the C501.

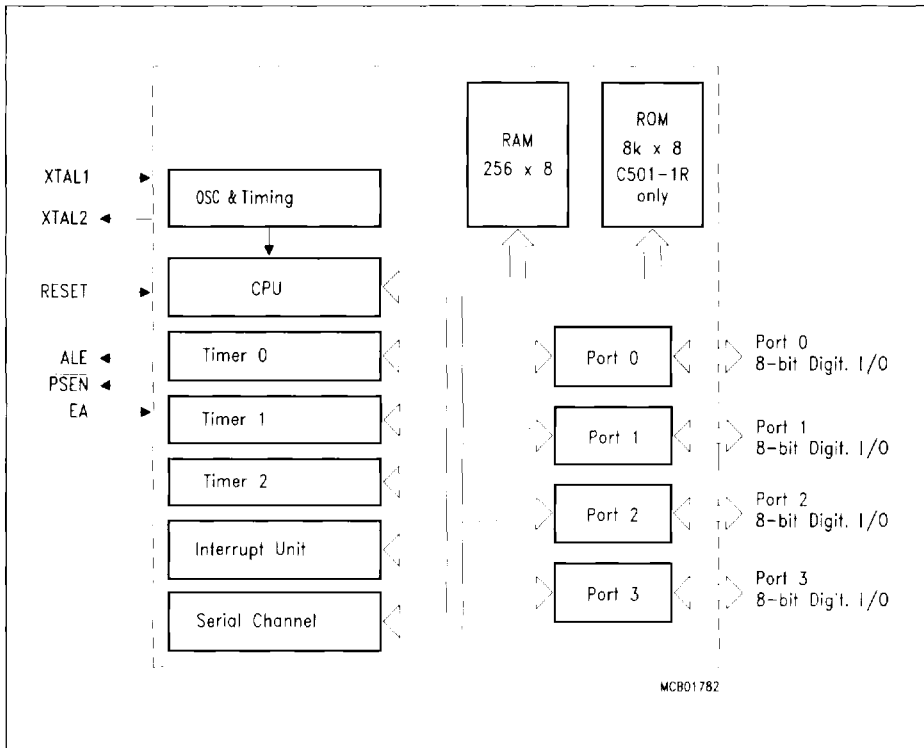


Figure 1
Block Diagram of the C501

CPU

The C501 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three- byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0µs (24 MHz: 500 ns, 40 MHz : 300 ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. D0 _H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag
AC	Auxiliary Carry Flag (for BCD operations)
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits
0 0	Bank 0 selected, data address 00 _H – 07 _H
0 1	Bank 1 selected, data address 08 _H – 0F _H
1 0	Bank 2 selected, data address 10 _H – 17 _H
1 1	Bank 3 selected, data address 18 _H – 1F _H
OV	Overflow Flag
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00_H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3**.

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the C501. **Table 3** illustrates the contents of the SFRs.

Table 1
Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	P0 ¹⁾	FFH	98H	SCON ¹⁾	00H
81H	SP	07H	99H	SBUF	XXH ²⁾
82H	DPL	00H	9AH	reserved	XXH ²⁾
83H	DPH	00H	9BH	reserved	XXH ²⁾
84H	reserved	XXH ²⁾	9CH	reserved	XXH ²⁾
85H	reserved	XXH ²⁾	9DH	reserved	XXH ²⁾
86H	reserved	XXH ²⁾	9EH	reserved	XXH ²⁾
87H	PCON	0XXX0000B ²⁾	9FH	reserved	XXH ²⁾
88H	TCON ¹⁾	00H	A0H	P2 ¹⁾	FFH
89H	TMOD	00H	A1H	reserved	XXH ²⁾
8AH	TL0	00H	A2H	reserved	XXH ²⁾
8BH	TL1	00H	A3H	reserved	XXH ²⁾
8CH	TH0	00H	A4H	reserved	XXH ²⁾
8DH	TH1	00H	A5H	reserved	XXH ²⁾
8EH	reserved	XXH ²⁾	A6H	reserved	XXH ²⁾
8FH	reserved	XXH ²⁾	A7H	reserved	XXH ²⁾
90H	P1 ¹⁾	FFH	A8H	IE ¹⁾	0X000000B ²⁾
91H	reserved	00H	A9H	reserved	XXH ²⁾
92H	reserved	XXH ²⁾	AAH	reserved	XXH ²⁾
93H	reserved	XXH ²⁾	ABH	reserved	XXH ²⁾
94H	reserved	XXH ²⁾	ACH	reserved	XXH ²⁾
95H	reserved	XXH ²⁾	ADH	reserved	XXH ²⁾
96H	reserved	XXH ²⁾	AEH	reserved	XXH ²⁾
97H	reserved	XXH ²⁾	AFH	reserved	XXH ²⁾

¹⁾ Bit-addressable Special Function Register

²⁾ X means that the value is indeterminate and the location is reserved

Table 1
Special Function Registers in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0_H	P3¹⁾	FF_H	D8_H	reserved	XX _H ²⁾
B1 _H	reserved	XX _H ²⁾	D9 _H	reserved	XX _H ²⁾
B2 _H	reserved	XX _H ²⁾	DA _H	reserved	XX _H ²⁾
B3 _H	reserved	XX _H ²⁾	DB _H	reserved	XX _H ²⁾
B4 _H	reserved	XX _H ²⁾	DC _H	reserved	XX _H ²⁾
B5 _H	reserved	XX _H ²⁾	DD _H	reserved	XX _H ²⁾
N6 _H	reserved	XX _H ²⁾	DE _H	reserved	XX _H ²⁾
B7 _H	reserved	XX _H ²⁾	DF _H	reserved	XX _H ²⁾
B8_H	IP¹⁾	XX000000_B²⁾	E0_H	ACC¹⁾	00_H
B9 _H	reserved	XX _H ²⁾	E1 _H	reserved	XX _H ²⁾
BA _H	reserved	XX _H ²⁾	E2 _H	reserved	XX _H ²⁾
BB _H	reserved	XX _H ²⁾	E3 _H	reserved	XX _H ²⁾
BC _H	reserved	XX _H ²⁾	E4 _H	reserved	XX _H ²⁾
BD _H	reserved	XX _H ²⁾	E5 _H	reserved	XX _H ²⁾
BE _H	reserved	XX _H ²⁾	E6 _H	reserved	XX _H ²⁾
BF _H	reserved	XX _H ²⁾	E7 _H	reserved	XX _H ²⁾
C0_H	reserved	XX _H ²⁾	E8_H	reserved	XX _H ²⁾
C1 _H	reserved	XX _H ²⁾	E9 _H	reserved	XX _H ²⁾
C2 _H	reserved	XX _H ²⁾	EA _H	reserved	XX _H ²⁾
C3 _H	reserved	XX _H ²⁾	EB _H	reserved	XX _H ²⁾
C4 _H	reserved	XX _H ²⁾	EC _H	reserved	XX _H ²⁾
C5 _H	reserved	XX _H ²⁾	ED _H	reserved	XX _H ²⁾
C6 _H	reserved	XX _H ²⁾	EE _H	reserved	XX _H ²⁾
C7 _H	reserved	XX _H ²⁾	EF _H	reserved	XX _H ²⁾
C8_H	T2CON	00_H	F0_H	B¹⁾	00_H
C9 _H	T2MOD	XXXXXXXX0 _B ²⁾	F1 _H	reserved	XX _H ²⁾
CA _H	RC2L	00 _H	F2 _H	reserved	XX _H ²⁾
CB _H	RC2H	00 _H	F3 _H	reserved	XX _H ²⁾
CC _H	TL2	00 _H	F4 _H	reserved	XX _H ²⁾
CD _H	TH2	00 _H	F5 _H	reserved	XX _H ²⁾
CE _H	reserved	XX _H ²⁾	F6 _H	reserved	XX _H ²⁾
CF _H	reserved	XX _H ²⁾	F7 _H	reserved	XX _H ²⁾
D0_H	PSW¹⁾	00_H	F8_H	reserved	XX _H ²⁾
D1 _H	reserved	XX _H ²⁾	F9 _H	reserved	XX _H ²⁾
D2 _H	reserved	XX _H ²⁾	FA _H	reserved	XX _H ²⁾
D3 _H	reserved	XX _H ²⁾	FB _H	reserved	XX _H ²⁾
D4 _H	reserved	XX _H ²⁾	FC _H	reserved	XX _H ²⁾
D5 _H	reserved	XX _H ²⁾	FD _H	reserved	XX _H ²⁾
D6 _H	reserved	XX _H ²⁾	FE _H	reserved	XX _H ²⁾
D7 _H	reserved	XX _H ²⁾	FF _H	reserved	XX _H ²⁾

¹⁾ Bit-addressable Special Function Register

²⁾ X means that the value is indeterminate and the location is reserved

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	E0H ¹⁾	00H
	B	B-Register	F0H ¹⁾	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	D0H ¹⁾	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	A8H ¹⁾	0X000000B ²⁾
	IP	Interrupt Priority Register	B8H ¹⁾	XX000000B ²⁾
Ports	P0	Port 0	80H ¹⁾	FFH
	P1	Port 1	90H ¹⁾	FFH ³⁾
	P2	Port 2	A0H ¹⁾	FFH
	P3	Port 3	B0H ¹⁾	FFH
Serial Channels	PCON ²⁾	Power Control Register	87H	0XXX0000B ²⁾
	SBUF	Serial Channel Buffer Reg.	99H	XXH ³⁾
	SCON	Serial Channel 0 Control Reg.	98H ¹⁾	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	88H ¹⁾	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	C8H ¹⁾	00H
	T2MOD	Timer 2 Mode Register	C9H	00H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CAH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
	Pow. Sav. Modes	PCON	Power Control Register	87H

¹⁾ Bit-addressable special function registers

²⁾ This special function register is listed repeatedly since some bits of it also belong to other functional blocks

³⁾ X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit 7	6	5	4	3	2	1	0
80 _H	P0								
81 _H	SP								
82 _H	DPL								
83 _H	DPH								
87 _H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88 _H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89 _H	TMOD	GATE	C/ \bar{T}	M1	M0	GATE	C/ \bar{T}	M1	M0
8A _H	TL0								
8B _H	TL1								
8C _H	TH0								
8D _H	TH1								
90 _H	P1								
98 _H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99 _H	SBUF								
A0 _H	P2								
A8 _H	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
B0 _H	P3								
B8 _H	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0
C8 _H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/ \bar{T} 2	CP/RL2
C9 _H	T2MOD	-	-	-	-	-	-	-	DCEN

--	--	--	--	--	--	--	--	--	--

 SFR bit and byte addressable

--	--	--	--	--	--	--	--	--	--

 SFR not bit addressable

- : = this bit location is reserved

Table 3
Contents of SFRs, SFRs in Numeric Order (cont'd)

Address	Register	Bit 7	6	5	4	3	2	1	0
CA _H	RC2L								
CB _H	RC2H								
CC _H	TL2								
CD _H	TH2								
D0 _H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0 _H	ACC								
F0 _H	B								

 SFR bit and byte addressable

 SFR not bit addressable

- : = this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in table 4:

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/\bar{T}	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{osc}/12 \cdot 32$	$f_{osc}/24 \cdot 32$
1	16-bit timer/counter	X	X	1	1	$f_{osc}/12$	$f_{osc}/24$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{osc}/12$	$f_{osc}/24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{osc}/12$	$f_{osc}/24$

In the "timer" function ($C/\bar{T} = '0'$) the register is incremented every machine cycle. Therefore the count rate is $f_{osc}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{osc}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

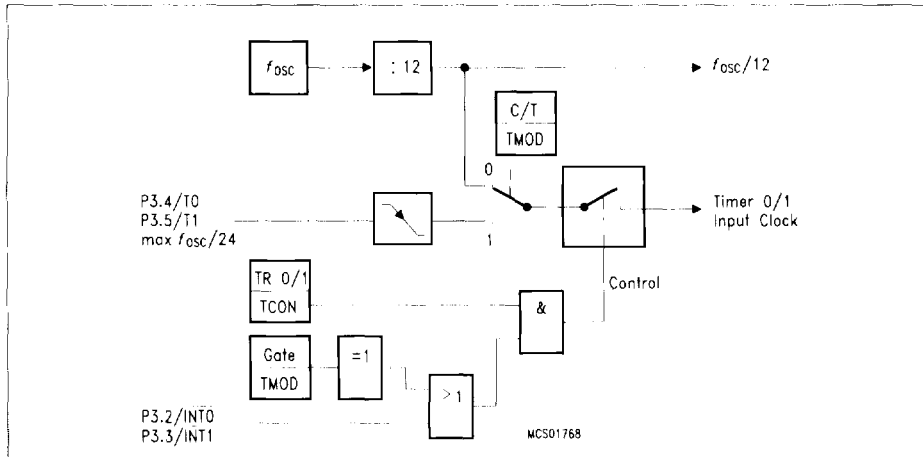


Figure 2
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit $C/\overline{T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON		P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/ RL2	TR2	DCEN	EXEN	internal			external (P1.0/T2)	
16-bit Auto- reload	0	0	1	0	0	X		reload upon overflow	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)			
	0	0	1	1	X	0	Down counting			
	0	0	1	1	X	1	Up counting			
16-bit Cap- ture	0	1	1	X	0	X		16 bit Timer/Counter (only up-counting)	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L			
Baud Rate Gene- rator	1	X	1	X	0	X		no overflow interrupt	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓	request (TF2) extra external interrupt ("Timer 2")			
off	X	X	0	X	X	X		Timer 2 stops	-	-

Note: ↓ =  falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 7**.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{osc}/12$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$f_{osc}/32$ or $f_{osc}/64$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0	$f_{osc}/12$
	2	$(2^{SMOD} \times f_{osc}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3	$(2^{SMOD} \times \text{timer 1 overflow rate}) / 32$
	1,3	$(2^{SMOD} \times f_{osc}) / (32 \times 12 \times (256 - TH1))$
Timer 2	1,3	$f_{osc} / (32 \times (65536 - (RC2H, RC2L)))$

Interrupt System

The C501 provides 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.

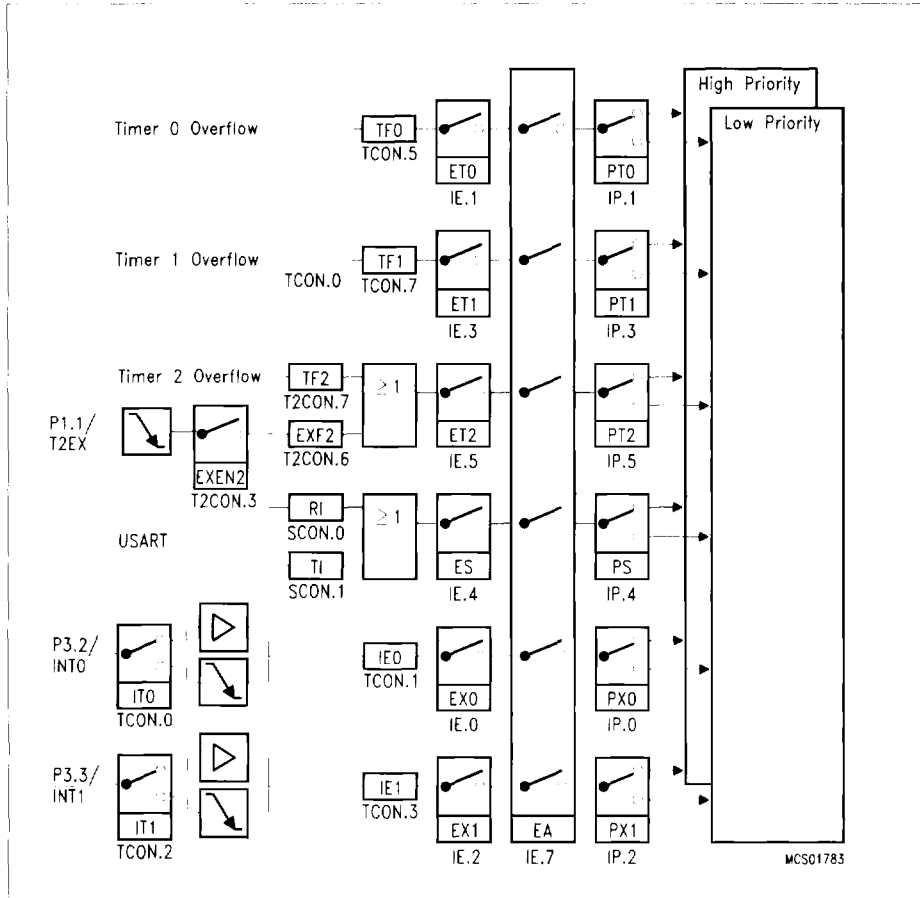


Figure 3
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003 _H
TF0	Timer 0 interrupt	000B _H
IE1	External interrupt 1	0013 _H
TF1	Timer 1 interrupt	001B _H
RI + TI	Serial port interrupt	0023 _H
TF2 + EXF2	Timer 2 interrupt	002B _H

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Priority-Within-Level

Interrupt Source	Priority
External Interrupt 0, Timer 0 Interrupt,	High
External Interrupt 1, Timer 1 Interrupt, Serial Channel,	↓
Timer 2 Interrupt,	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	<ul style="list-style-type: none"> - enabled interrupt - Hardware Reset 	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	- 40 to + 85 °C
Storage temperature (T_{ST}).....	- 65 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	- 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....	- 0.5 V to $V_{CC} + 0.5$ V
Input current on any pin during overload condition.....	- 10 mA to + 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation.....	TBD

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

$V_{CC} = 5\text{ V} + 10\% , -15\%$; $V_{SS} = 0\text{ V}$;

$T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ for the SAB-C501

$T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except \overline{EA} , RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	-
Input low voltage (\overline{EA})	V_{IL1}	-0.5	$0.2 V_{CC} - 0.3$	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, \overline{EA} , RESET)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to \overline{EA} , RESET	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	$I_{OL} = 1.6\text{ mA}^{1)}$
Output low voltage (port 0, ALE, PSEN)	V_{OL1}	-	0.45	V	$I_{OL} = 3.2\text{ mA}^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	-	V	$I_{OH} = -80\text{ }\mu\text{A}$, $I_{OH} = -10\text{ }\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 $0.9 V_{CC}$	-	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$, $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45\text{ V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	μA	$V_{IN} = 2\text{ V}$
Input leakage current (port 0, \overline{EA})	I_{li}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$
Power supply current:					
Active mode, 12 MHz ⁷⁾	I_{CC}	-	21	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 12 MHz ⁷⁾	I_{CC}	-	4.8	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Active mode, 24 MHz ⁷⁾	I_{CC}	-	36.2	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 24 MHz ⁷⁾	I_{CC}	-	8.2	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Active mode, 40 MHz ⁷⁾	I_{CC}	-	56.5	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 40 MHz ⁷⁾	I_{CC}	-	12.7	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Power Down Mode	I_{PD}	-	50	μA	$V_{CC} = 2 \dots 5.5\text{ V}^{3)}$

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the $0.9 V_{CC}$ specification when the address lines are stabilizing.
- 3) I_{PD} (Power Down Mode) is measured under following conditions:
 $\overline{EA} = \text{Port0} = V_{CC}$; $\text{RESET} = V_{SS}$; $\text{XTAL2} = \text{N.C.}$; $\text{XTAL1} = V_{SS}$; all other pins are disconnected.
- 4) I_{CC} (active mode) is measured with:
 XTAL1 driven with $t_{CL,CH}, t_{CH,CL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; $\text{XTAL2} = \text{N.C.}$;
 $\overline{EA} = \text{Port0} = \text{RESET} = V_{CC}$; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with $t_{CL,CH}, t_{CH,CL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; $\text{XTAL2} = \text{N.C.}$;
 $\text{RESET} = \overline{EA} = V_{SS}$; $\text{Port0} = V_{CC}$; all other pins are disconnected;
- 7) $I_{CC, \text{max}}$ at other frequencies is given by:
 active mode: $I_{CC} = 1.27 \times f_{OSC} + 5.73$
 idle mode: $I_{CC} = 0.28 \times f_{OSC} + 1.45$
 where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5 \text{ V}$.